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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/678,163	10/02/2000	Jerry D. Kline	1303-1008	4116

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 05/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action	Application No.	Applicant(s)	
	09/678,163	KLINE, JERRY D.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 23 April 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

a) ☐ The period for reply expires _____months from the mailing date of the final rejection.

b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1.☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.

2.☒ The proposed amendment(s) will not be entered because:

(a) ☒ they raise new issues that would require further consideration and/or search (see NOTE below);

(b) ☐ they raise the issue of new matter (see Note below);

(c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or

(d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: *See Continuation Sheet.*

3.☐ Applicant's reply has overcome the following rejection(s): _____.

4.☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

5.☐ The a)☐ affidavit, b)☐ exhibit, or c)☐ request for reconsideration has been considered but does NOT place the application in condition for allowance because: _____.

6.☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.

7.☐ For purposes of Appeal, the proposed amendment(s) a)☐ will not be entered or b)☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: _____.

Claim(s) withdrawn from consideration: _____.

8.☐ The proposed drawing correction filed on _____ is a)☐ approved or b)☐ disapproved by the Examiner.

9.☐ Note the attached Information Disclosure Statement(s)(PTO-1449) Paper No(s). _____.

10.☐ Other: _____

W. DAVID COLEMAN
PRIMARY EXAMINER

Continuation of 2. NOTE: The newly added limitations " to determine inculsion in the matches set " raise new issues that require further consideration and/or search.

The Attachment to Advisory Action

Response to Arguments

Applicant's arguments filed 10/23/02 have been fully considered but they are not persuasive for the reasons as follows.

Applicant's argument is on the ground that the electrical testing of Razon "occurs prior to the implementation of the interposers 106 of figure 2B" because Razon teaches performing an electrical testing prior to the integration of the devices 101. Accordingly, applicant asserts that Razon neither discloses nor suggests simultaneously testing at least two of the integrated circuit chips of the semiconductor wafer.

In response to the argument, applicant's attention is directed to examine the exact meanings of the phrase "prior to the integration of the devices 101" in lights of the related text. Obviously, the applicant intends to interpret that interposers 106 are electrically tested first (i.e. before the step of Fig.2B) and then are attached over each individual chip 100a, 100b etc. on the portion of the semiconductor wafer 100 as shown in Fig. 2B.

To clarify this issue, it is necessary to compare Fig. 2B with Fig. 2F in lights of the related text. The phrase "performing an electrical testing prior to the integration of the devices 101" means performing the electrical testing prior to the integration of ***an encapsulated chip package*** **101 as shown in Fig. 2F,** not prior to the integration of the interposers 106 of Figure 2**B** (col. 6, lines 55-59). In other words, the phrase merely indicates that the timing of the electrical testing occurs any time prior to forming the encapsulated chip package 101 but not necessary as early as prior to attaching the interposers 106 over the individual chip 100a, 100b etc. This is

quite different from the applicant's assertion that " testing occurs prior to the implementation of the interposers 106 of figure 2B." (at the middle of page 15)

In fact, Razon et al. on column 4, lines 42-47, clearly states that " Prior to the integration of the devices 101, each chip on wafer 100 is tested using conventional electrical test equipment, and any defective chips are identified. " and that " The tests determine whether **each individual chips 100a, 100b etc.** on the portion of the semiconductor wafer 100 complies with a predetermined set of acceptance criteria." (emphasis added) In other words, the electrical test is an acceptance test with respect to each individual chips 100a, 100b etc. If the testing occurred prior to the attachment of the interposers 106 of figure 2B, how each individual chips 100a, 100b etc would be electrically tested because the interposers 106 of figure 2B have NOT been electrically and mechanically coupled to the chips 100a, 100b etc yet.

In addition, since interposers 106 are electrically and mechanically coupled to each individual chips 100a, 100b, etc on the **entire** wafer 100 as shown in Fig. 2B, the test is performed on a **wafer level**. Particularly, Razon et al. on column 4, lines 29-31 teach the microball grid array process is performed at wafer-level.

Applicant further argues that the deficiency of Lam reference is not cured by applicant's admitted prior art (hereinafter referred as " AAPA") because AAPA teaches selecting at least two of the chip assemblies for inclusion in a matched set based upon the individual testing.

In response to the argument, Lam substantially teaches the claimed invention, including electrically and mechanically coupling a semiconductor wafer 21 having a plurality of integrated circuit chips 25 to an interposer 31 to form a wafer-interposer assembly 39; simultaneously testing at least two of the integrated circuit chips 25 of the semiconductor wafer 21, i.e. multiple

chips 25 are on the single wafer 21 but are not diced until the packaging operation on the single wafer 21 has been completed; and the interposer substrate 31 can be approximately the same size as the wafer 21 and is coupled to the wafer 21 (col. 4, lines 53-54), i.e. when multiple chips 25 are under testing they are tested at the same time because multiple chips 25 are on the single wafer 21 and are tested before they are diced into plural chip assemblies 70 and 72; and then dicing the wafer-interposer assembly 39 into a plurality of chip assemblies such as 70 and 72 (col. 5, line 24-26).

Lam does not expressly teach selecting at least two of the chip assemblies for inclusion in the matched set based upon the simultaneously testing.

AAPA teaches that, in semiconductor packing process, one approach for improving overall system performance is through the use of matched sets, i.e. by sorting several identical or dissimilar components that have been identified by testing and assembly together as a matched set. (pages 2-3).

Therefore, one of the ordinary skill in the art would have been motivated to select at least two of the chip assemblies for inclusion in the matched set as taught by AAPA based upon the simultaneously testing of Lam since by doing so it would enhance the overall system performance (AAPA on page 2).

For the reasons above, 102(e) and 103(a) rejections as set forth in the Final rejection are deemed proper.

Hsien Ming Lee

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Technology Center 2800